# Assignment 1

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Indholdsfortegnelse

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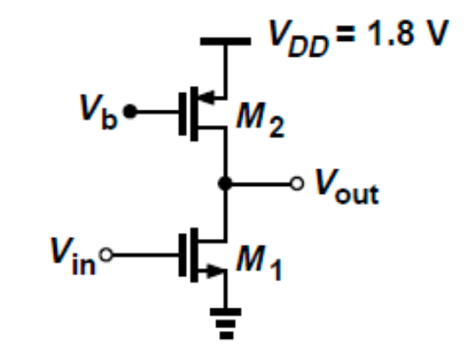
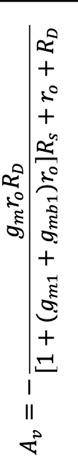
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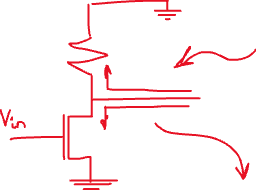
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## Prerequisites

Throughout this assignment I will be setting the body of each transistor to ground if nothing else is said.

## Question 1. CS configuration and transistor values.

The CS stage of Fig.1 must provide a voltage gain of 10 with a bias current of 0.5 mA.

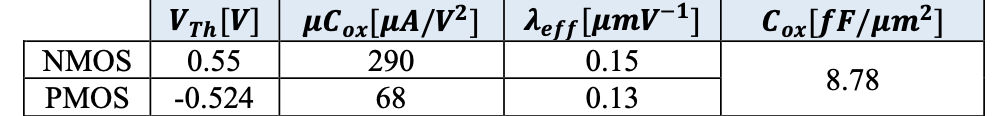


### Calculate the required value of

Setting all sources to ground except for Vin:

For small signal we work in saturation

Focusing on just the magnitude of the current:

Saying

Taking values from the cheat sheet. And with the bias current.

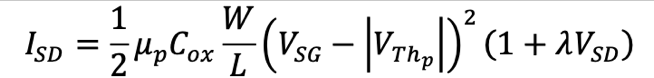
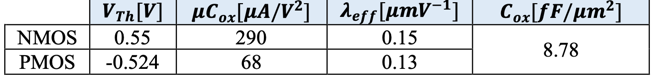
Working with integer values of unit width, the width should be atleast 11.

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### Calculate the required Vb if is 20/0.18

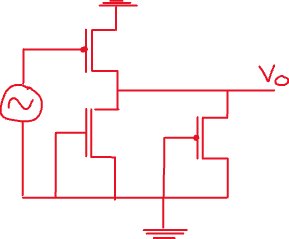
For this to work I want to stay in saturation region:

If this is fullfilled the following is true:

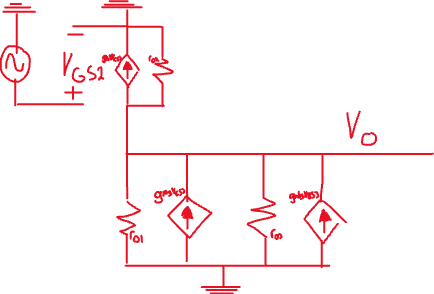
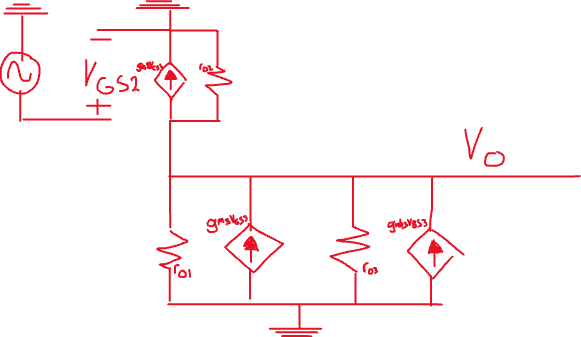
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The channel length modulation made it non constant, leaving us with a expression of Vout.

## Question 2. Determine the voltage gain of the stage shown I Fig. 2, Assume .

My small signal   
circuit:



And it’s equivalent circuit using  
the hybrid pi model



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## Question 3. Boundaries and Intrinsic gain.

A mosfet when used as an amplifier is typically operated in the saturation region, and a large intrinsic gain is desirable

### Explain why there is an optimal gate bias voltage to maximize the mosfet transconductance

Let me look at an equation for gm.

For nmos  
   
For nmos.   
  
Both under the assumption that it’s the current from the transistors being in saturation region, that we want to describe, as we usually want with small signal.   
Let’s look at the nmos:

This means, that is proportional to . But this is assumes, that we are in the saturation region, when nearing the edge of this region, the equation becomes more and more unvalid.

It’s bounds are:

================================================================  
So if the goal is to maximize the transconductance , Setting to be equal to  
 would maximize gm while still being in saturation region.   
A little less would probably work better too, for a real life problem.  
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### Does intrinsic gain degrade with decreasing channel length L. Give reason for your answer.

So as I derived last time, decreasing the channel length L would have had a negative proportinal effect on the drain source current.

Now looking at it as a whole:

Where   
So let’s put it together.



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So for the question. Does the intrinsic gain degrade with decreasing channel length L, the answer is yes, as the intrinsic gain is proportional to the channel length L.   
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## Question 4. Body effect free

If you want your design to be “Body Effect” free, which type of MOSFET will you prefer and why?

If I wanted a “Body effect free” mosfet I would use a NMOS.  
And the reason why is that it’s source is usually set to ground, which if I were to not set my voltages at body equal to the source, setting it to ground would have resulted in the same thing for the NMOS.   
That’s because we usually tie NMOS to the pulldown network and PMOS for the pull up network.

For a pmos setting the body to ground, with it having source at VDD would result in:

This is for the large signal analysis though, but it does matter.

## Question 5. Voltage gain with CS configuration.

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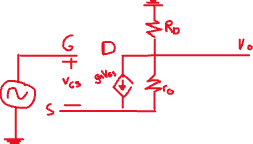
Automatisk genereret beskrivelseEt billede, der indeholder tekst, skærmbillede, Font/skrifttype, linje/række

Automatisk genereret beskrivelseThe CS stage of Fig. 4 carries a bias current of 1mA. If and , compute the required value of (W/L) for a gate voltage of 1V. What is the voltage gain of the circuit?

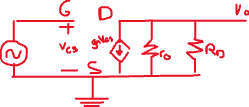


Setting the gate source voltage to

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Let me derive the gain:



Now simplified:   
The small signal model   
for my circuit:



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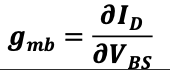
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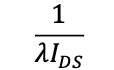
Seems small. Can’t remember if we want this characteristics off of CS configuration.   
For SF we want a gain from 0 -> 1, but for this? I don’t know right now.

## Question 6.

## Et billede, der indeholder Font/skrifttype, diagram, linje/række, design Automatisk genereret beskrivelseQuestion 11. Cascode

The MOS cascode of the circuit below must provide a bias current of 0.5 mA with an output impedance of at least 50k. If μnCox=100μA/V2 and (W/L) = 20/0.18 for both transistors, compute the maximum tolerable value of λ



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Automatisk genereret beskrivelseEt billede, der indeholder Font/skrifttype, diagram, linje/række, design

Automatisk genereret beskrivelseSwitching the symbols, as my formula for had the symbols opposite of what this circuit looks like.

If the m2 body is set to source of m2, which would simplify this case:

With the same ratio, the channel lambda should be the same as well.



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So for the output resistanse to be of atleast 50kΩ, then the maximum tolerable   
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